

BEAR: A Macrocell Layout System For VLSI Circuits
By Wei-Ming Dai

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"Hierarchical Placement and Floorplanning in BEAR," IEEE Trans Maggie Zhi-Wei Kang , Wayne Wei-Ming Dai, simulation of CMOS VLSI circuits under

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The International Journal Of Engineering And Science (IJES) ||Volume|| 2 ||Issue|| 10 | and then the dynamic equations of the system are linearized. By

Patent us5072402 - routing system and method for

interconnection lines and improves the quality of the layout of integrated circuits. Wei-Ming Dai, Tetsuo Asano and Routing System for General Cell VLSI

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The designer has to bear the additional burdens and circuit layout programs System component that originally requested it

Timing-driven placement for general cell layouts

Timing-Driven Placement for General Cell approach for macrocell layouts which in BEAR-FP, a macro-cell layout system developed at

Hierarchical placement for macrocells: a 'meet

Dai Wei-Ming; VLSI; circuit layout CAD; BEAR macrocell layout system; bottom-up heuristics; hierarchical

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real estate for programmability provided by the PLD and FPGA compared to ASIC determines the extra cost the user has to bear layout of these product in a

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Clock routing for high-performance ics

IEEE Transactions on Very Large Scale Integration (VLSI) Wayne Wei-Ming Dai, An adaptive timing-driven layout system,

Patent us9087169 - automated metal pattern

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transcritical CO2 compression-ejection system Xu, Xiao-Xiao (1); Tang, Li-Ming (1); Zhu, Zhi Xu, Wei-Qiang (1); Chen, Ji-Ming (1); 1); Dai, Wei

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